**REMARKS**

Entry of this Amendment in accordance with the provisions of 37 CFR §1.114 is respectfully requested, noting that this Amendment is filed as a Submission with a Request for Continued Examination on even date herewith.

By the present amendment, the claims 18, 19, 26, and 27 have been amended to respond to the 35 USC §112 first and second paragraph rejections. With regard to claims 18, 19, 26 and 27, these claims have been amended to provide clear antecedent basis, noting that the use of the term "multilayer wiring substrate" instead of "multilayer wiring board" was an inadvertent error. As to the rejection concerning the relative thermal conductivity in claim 27, the claim has been amended to clearly define that:

> "said through holes in the multilayer wiring board having formed on sides or inside thereof a conductive material, different than a material comprising the multilayer wiring board, said conductive material having a higher thermal conductivity than a thermal conductivity of the material comprising the multilayer wiring board."

It is noted that this corresponds to the material shown, for example, in the figures of the present application labeled with the numeral 4, that is, the material provided in the thermal vias 4 of the illustrated structure. As discussed in paragraph [0044], for example, the thermal cavities 4 are filed with a material with high thermal conductivity to provide good thermal conduction and reduced thermal resistance between heating areas in the semiconductor device 1 and the back of the wiring board 3. As noted in paragraph [0056] for example:

> "thermal vias 4 are arranged on the multilayer wiring board 3 similarly to via holes 5, side surfaces of the thermal vias 4 are formed with a layer of a material, which is thermally and electrically conductive, or interiors of the thermal vias 4 are filled with a material, which is thermally and electrically conductive."

In the Office Action, it is stated:

> "particularly, the multilayer wiring board comprises the material, therefore, it is unclear how the material can have higher thermal conductivity than the multilayer wiring board."

By virtue of the present amendment, it is clarified that there is conductive material, such as used on the sidewalls or inside the thermal vias 4, which is different than the material

used to comprise the multilayer wiring board 3. Therefore, it is respectfully submitted that the amended claim language clarifies this matter, and, correspondingly, reconsideration and removal of the 35 USC §112, first and second paragraph, rejections is respectfully requested.

Reconsideration and removal of the 35 USC §102 and §103 rejections set forth in the Office Action against all of the claims based on either Hayasaka (USP 6,809,421) alone, or the admitted prior art alone, or in combination with one another is also respectfully requested. With regard to this, it is respectfully submitted that the Office Action incorrectly focuses on the concept that the through hole in the silicon dies disclosed in Figs. 7-25 of Hayasaka have an equal effect to the thermal vias, and that, in the mounting structure shown in Figs. 4, 5, 23 and 26-33 of Hayasaka, for example, the through holes and the solder bumps are arranged at the same level of position in a two-dimensional view. It is respectfully submitted that this is not an accurate portrayal of Hayasaka, and that the through holes of Hayasaka are not arranged and do not operate in the same manner as the thermal vias of the claimed invention.

In particular, as previously discussed in the Amendment filed on August 12, 2009, the flow of heat in the claimed structure is completely different than that taught by Hayasaka. In particular, in Hayasaka, although it is not clear which surface of a silicon chip is the circuit forming chip, it appears that, from Figs. 6 through 9, that a face-up structure is provided (noting that, for example, in Fig. 4 the devices are formed on the upper surface of the silicon dies 2, immediately under an interconnection layer 3. However, regardless of whether the arrangement in Hayasaka is a face-up arrangement or a flip chip arrangement, the heat generated in the circuit three dimensionally expands into the silicon element, and transfers in the horizontal direction of the drawings. The reason for this is that, except for the bump 8 shown in Fig. 4, there is no arrangement for transferring heat to another layer. With regard to this, it is noted that spaces are provided between the chips in Hayasaka, such that the entirety of the heat generated in the devices expands in the surface direction of the chip and then is radiated through the solder pump, which is entirely different than the flow of heat utilizing the thermal vias in the claimed invention.

In particular, in the present claimed invention, most of the heat diffuses and expands in a downward direction of the chip, and flows from the emitter wiring through the via hole to the thermal via in the board. This is a completely different arrangement than that taught by Hayasaka.

**REQUEST FOR INTERVIEW**

Prior to taking up this application for examination, before the end of the three-month suspension period, it is requested that the Examiner contact the undersigned attorney so that an interview can be conducted with regard to this application. Applicants and the undersigned attorney greatly appreciate the examiner's courtesy with regard to this.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 500.40530X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
**ANTONELLI, TERRY, STOUT & KRAUS, LLP**

GEM/dks
Appendix

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